REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02; editorial changes throughout. Redrawn.	93-06-23	M. A. Frye
B	Update boilerplate. Add device types 03 and 04. Add case outline M. Editorial changes throughout.	94-06-30	M. A. Frye

REV																			
SHEET																			
REV	**B**	**B**																	
SHEET	**15**	**16**																	

REV STATUS OF SHEETS	**REV**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**
	SHEET	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-06-23

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS,
FIELD PROGRAMMABLE GATE ARRAY,
2000 GATES, MONOLITHIC SILICON

SIZE	**CAGE CODE**	
A	**67268**	**5962-90965**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	90965	01	M	X	X
Federal stock class designator	RHA designator (See 1.2.1)		Device type (See 1.2.2)	Device class designator (See 1.2.3)	Case outline (See 1.2.4)	Lead finish (See 1.2.5)
_____ Drawing number _____/						

1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Bin speed
01	1020A	2000 gate, field programmable gate array	186 ns
02	1020A-1	2000 gate, field programmable gate array	158 ns
03	1020B	2000 gate, field programmable gate array	168.2 ns
04	1020B-1	2000 gate, field programmable gate array	142.9 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CQCC2 - J44	44	J-lead chip carrier
Y	CQCC2 - J68	68	J-lead chip carrier
Z	CQCC2 - J84	84	J-lead chip carrier
U	CMGA15 - PN	84	Pin grid array 1/
T	CQCC1 - F84	84	Unformed lead chip carrier
M	See figure 1	84	Unformed lead chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Actual number of pins is 85 including one index or orientation pin (C3).

1.3 Absolute maximum ratings. 2/

DC supply voltage range (V_{DD})	-0.5 V dc to +7.0 V dc
Input voltage range (V_I)	-0.5 V dc to V_{DD} + 0.5 V dc
Output voltage range (V_O)	-0.5 V dc to V_{DD} + 0.5 V dc
I/O source sink current I_{IO})	±20 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Case outline M	10°C/W 3/
Maximum junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
4/ When a QML source exists, a value shall be provided.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standard Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Procedures from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with figure 1 and 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table.

3.2.3.1 Unprogrammed devices. The truth table or test vectors for unprogrammed devices for contracts involving no altered item drawing is not part of this drawing. When required in screening (see 4.2 herein) or quality conformance inspection group A, B, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of logic modules shall be utilized or at least 25 percent of the total logic modules shall be utilized for any altered item drawing pattern.

3.2.3.2 Programmed devices. The truth table or test vectors for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-I-38535, appendix A).

3.11 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract.

3.11.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.11.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ 1/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output low voltage	V_{OL}	test one output at a time, $V_{DD} = 4.5\ V$, $I_{OL} = 4.0\ mA$		1,2,3	All		0.4	
Output high voltage	V_{OH}	test one output at a time, $V_{DD} = 4.5\ V$, $I_{OH} = -3.2\ mA$		1,2,3	All	3.7		V
Input low voltage	V_{IL}			1,2,3	All		0.8	V
Input high voltage	V_{IH}			1,2,3	All	2.0		V
Standby supply current	I_{DD}	outputs unloaded, $V_{DD} = 5.5\ V$, $V_{IN} = V_{DD}$ or GND		1,2,3	All		25	mA
Input leakage current	I_{IL}	$V_{DD} = 5.5\ V$, $V_{IN} = V_{DD}$ or GND		1,2,3	All	-10	10	µA
Output leakage current	I_{OZ}	$V_{DD} = 5.5\ V$, $V_{OUT} = V_{DD}$ or GND		1,2,3	All	-10	10	µA
Output short circuit current	I_{OS}	2/	$V_{OUT} = VDD$	1,2,3	01,02	20	140	mA
			$V_{OUT} = GND$	1,2,3	01,02	-10	-100	
I/O terminal capacitance	$C_{I/O}$	See 4.4.1c, f = 1.0 Mhz, $V_{OUT} = 0\ V$		4	All		20	pF
Functional tests	FT 3/	$V_{DD} = 4.5\ V$, See 4.4.1e, f		7,8A,8B	All			
Binning circuit delay	t_{PBLH}, t_{PBHL}	See figure 3, $V_{IL} = 0\ V$, $V_{IH} = 3.0\ V$, $V_{DD} = 4.5\ V$, $V_{OUT} = 1.5\ V$ 4/		9,10,11	01 02 03 04		186 158 168.2 142.9	ns

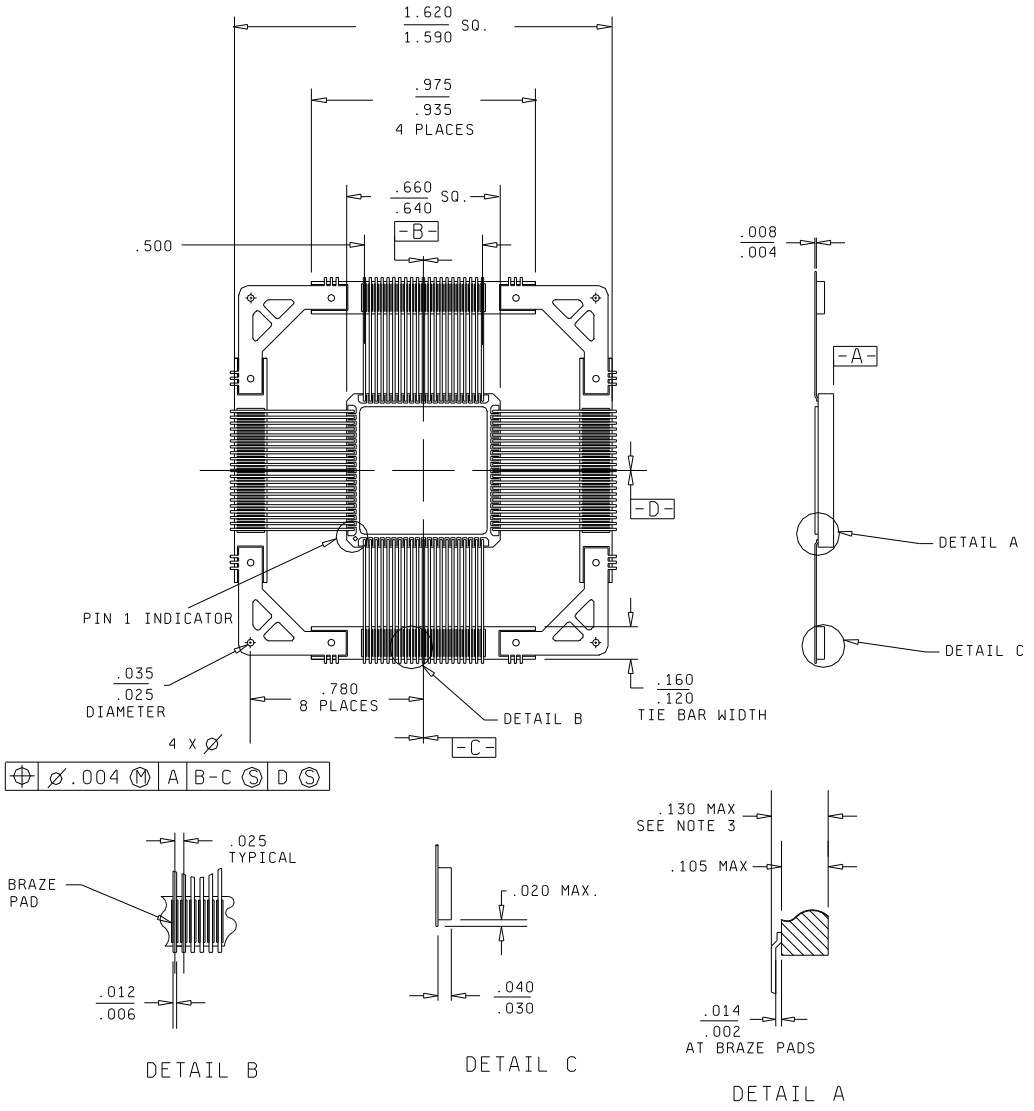
1/ All tests shall be performed under the worst case condition unless otherwise specified.

2/ $V_{DD} = 4.5\ V$ for minimum limits and $V_{DD} = 5.5\ V$ for maximum limits. Test one output at a time, duration of short circuit condition shall not exceed one second. This test for devices 01 and 02 only.

3/ Devices are functionally tested using a serial scan test method. Data is shifted into the SDI pin and the DCLK pin is used as a clock. The data is used to drive the inputs of the internal logic and I/O modules, allowing a complete functional test to be performed. The outputs of the module can be read by shifting out the output response or by monitoring the PRA and PRB pins. These tests form a part of the manufacturer's test tape and shall be maintained and available at the approved source(s) of supply upon request by DESC or the OEM.

4/ Binning circuit delay is defined as the input-to-output delay of a special path called the "binning circuit". The binning circuit shall be programmed into all device prior to screening. The binning circuit consists of one input buffer plus 28 logic modules plus one output buffer. The logic modules are distributed along two sides of the device. These modules are configured as inverting and non-inverting buffers and are connected through programmed antifuses with typical capacitive loading.

Case M



Inches	mm	Inches	mm	Inches	mm	Inches	mm
.002	.050	.020	2.67	.120	3.05	.935	23.75
.004	.100	.025	3.05	.130	3.30	.975	24.77
.006	.150	.030	3.30	.160	4.06	1.590	40.39
.008	.200	.035	4.06	.500	12.70	1.620	41.15
.012	.300	.040	12.70	.640	16.26		
.014	.360	.105	16.26	.660	16.76		

NOTES:
1. Dimensions are in inches.
2. The US goverment preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
3. For detail A: Includes lead attach dogleg height and lid height, whichever is greater.

FIGURE 1. Case outline.

Device type	All		All	All	
Case outlines	X	Y	Case outlines	X	Y
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	I/O	I/O	35	VDD	I/O
2	I/O	I/O	36	SDI or I/O	I/O
3	VDD	I/O	37	DCLK or I/O	I/O
4	I/O	VDD	38 1/	PRA or I/O	VDD
5	I/O	I/O	39 1/	PRB or I/O	I/O
6	I/O	I/O	40	I/O	I/O
7	I/O	I/O	41	I/O	I/O
8	I/O	I/O	42	I/O	I/O
9	I/O	I/O	43	GND	I/O
10	GND	I/O	44	I/O	I/O
11	I/O	I/O	45	- - -	I/O
12	I/O	I/O	46	- - -	I/O
13	I/O	I/O	47	- - -	I/O
14	VDD	GND	48	- - -	I/O
15	I/O	GND	49	- - -	GND
16	VPP	I/O	50	- - -	I/O
17	I/O	I/O	51	- - -	I/O
18	I/O	I/O	52	- - -	CLK or I/O
19	I/O	I/O	53	- - -	I/O
20	I/O	I/O	54	- - -	MODE
21	GND	VDD	55	- - -	VDD
22	I/O	I/O	56	- - -	SDI or I/O
23	I/O	I/O	57	- - -	DCLK or I/O
24	I/O	I/O	58 1/	- - -	PRA of I/O
25	VDD	VPP	59 1/	- - -	PRB or I/O
26	I/O	I/O	60	- - -	I/O
27	I/O	I/O	61	- - -	I/O
28	I/O	I/O	62	- - -	I/O
29	I/O	I/O	63	- - -	I/O
30	I/O	I/O	64	- - -	I/O
31	I/O	I/O	65	- - -	I/O
32	GND	GND	66	- - -	GND
33	CLK or I/O	I/O	67	- - -	I/O
34	MODE	I/O	68	- - -	I/O

1/ PRA and PRB are inverting signals for device types 01 and 02, and non-inverting signals for device types 03 and 04. PRA and PRB are used only for device testing or debugging. In normal operation, all device types exhibit identical logic on these pins.

FIGURE 2. Terminal connections.

Device type	All	Device type	All
Case outlines	Z	Case outlines	Z
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I/O	43	I/O
2	I/O	44	I/O
3	I/O	45	I/O
4	VDD	46	VDD
5	I/O	47	I/O
6	I/O	48	I/O
7	I/O	49	I/O
8	I/O	50	I/O
9	I/O	51	I/O
10	I/O	52	I/O
11	I/O	53	I/O
12	NC	54	I/O
13	I/O	55	I/O
14	I/O	56	I/O
15	I/O	57	I/O
16	I/O	58	I/O
17	I/O	59	I/O
18	GND	60	GND
19	GND	61	GND
20	I/O	62	I/O
21	I/O	63	I/O
22	I/O	64	CLK or I/O
23	I/O	65	I/O
24	I/O	66	MODE
25	VDD	67	VDD
26	VDD	68	VDD
27	I/O	69	I/O
28	I/O	70	I/O
29	I/O	71	I/O
30	I/O	72	SDI or I/O
31	I/O	73	DCLK or I/O
32	I/O	74 1/	PRA of I/O
33	VPP	75 1/	PRB or I/O
34	I/O	76	I/O
35	I/O	77	I/O
36	I/O	78	I/O
37	I/O	79	I/O
38	I/O	80	I/O
39	I/O	81	I/O
40	GND	82	GND
41	I/O	83	I/O
42	I/O	84	I/O

1/ PRA and PRB are inverting signals for device types 01 and 02, and non-inverting signals for device types 03 and 04. PRA and PRB are used only for device testing or debugging. In normal operation, all device types exhibit identical logic on these pins.

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All
Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	I/O	F9	CLK or I/O
A2	I/O	F10	GND
A3	I/O	F11	I/O
A4	I/O	G1	I/O
A5	I/O	G2	VDD
A6	I/O	G3	I/O
A7	I/O	G9	I/O
A8	I/O	G10	GND
A9	I/O	G11	I/O
A10	I/O	H1	I/O
A11 1/	PRA or I/O	H2	I/O
B1	I/O	H10	I/O
B2	NC	H11	I/O
B3	I/O	J1	I/O
B4	I/O	J2	I/O
B5	VDD	J5	I/O
B6	I/O	J6	I/O
B7	GND	J7	I/O
B8	I/O	J10	I/O
B9	I/O	J11	I/O
B10 1/	PRB or I/O	K1	I/O
B11	SDI or I/O	K2	VPP
C1	I/O	K3	I/O
C2	I/O	K4	I/O
C3	Keying pin	K5	GND
C5	I/O	K6	I/O
C6	I/O	K7	VDD
C7	I/O	K8	I/O
C10	DCLK or I/O	K9	I/O
C11	I/O	K10	I/O
D1	I/O	K11	I/O
D2	I/O	L1	I/O
D10	I/O	L2	I/O
D11	I/O	L3	I/O
E1	I/O	L4	I/O
E2	GND	L5	I/O
E3	GND	L6	I/O
E9	VDD	L7	I/O
E10	VDD	L8	I/O
E11	MODE	L9	I/O
F1	VDD	L10	I/O
F2	I/O	L11	I/O
F3	I/O		

1/ PRA and PRB are inverting signals for device types 01 and 02, and non-inverting signals for device types 03 and 04. PRA and PRB are used only for device testing or debugging. In normal operation, all device types exhibit identical logic on these pins.

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All
Case outline	T, M	Case outline	T, M
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	43	I/O
2	I/O	44	I/O
3	I/O	45	I/O
4	I/O	46	I/O
5	I/O	47	I/O
6	I/O	48	I/O
7	GND	49	GND
8	GND	50	GND
9	I/O	51	I/O
10	I/O	52	I/O
11	I/O	53	CLK/I/O
12	I/O	54	I/O
13	I/O	55	MODE
14	VDD	56	VDD
15	VDD	57	VDD
16	I/O	58	I/O
17	I/O	59	I/O
18	I/O	60	I/O
19	I/O	61	SDI/I/O
20	I/O	62	DCLK/I/O
21	I/O	63 1/	PRA/I/O
22	VPP	64 1/	PRB/I/O
23	I/O	65	I/O
24	I/O	66	I/O
25	I/O	67	I/O
26	I/O	68	I/O
27	I/O	69	I/O
28	I/O	70	I/O
29	GND	71	GND
30	I/O	72	I/O
31	I/O	73	I/O
32	I/O	74	I/O
33	I/O	75	I/O
34	I/O	76	I/O
35	VDD	77	VDD
36	I/O	78	I/O
37	I/O	79	I/O
38	I/O	80	I/O
39	I/O	81	I/O
40	I/O	82	I/O
41	I/O	83	I/O
42	I/O	84	I/O

NC = No connection

1/ PRA and PRB are inverting signals for device types 01 and 02, and non-inverting signals for device types 03 and 04. PRA and PRB are used only for device testing or debugging. In normal operation, all device types exhibit identical logic on these pins.

FIGURE 2. Terminal connections - Continued.

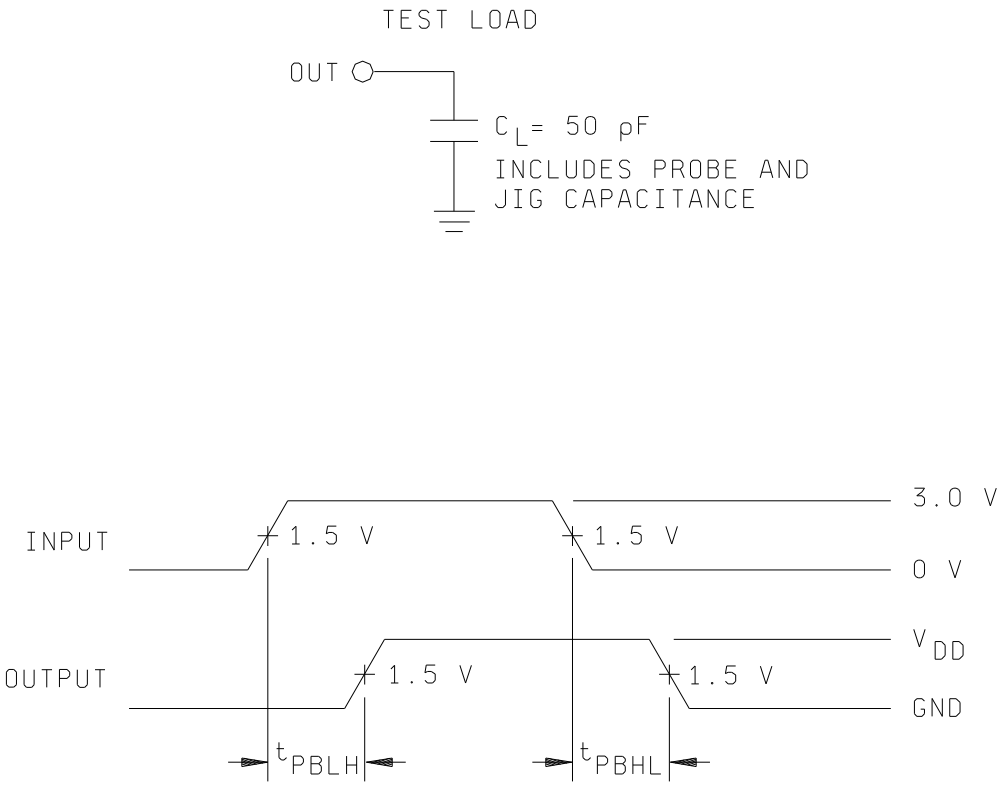


FIGURE 3. Switching test circuit and waveforms.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. A sample size of 5 devices with no failures, and all input and output terminals shall be required.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Programmed device (see 3.2.3.2) - For device class M, subgroups 7 and 8 tests shall consist of verifying the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device, these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

f. Unprogrammed devices shall be tested for programmability and dc and ac performance compliance to the requirements of group A, subgroups 1, 2, 3, 9, 10, and 11.

(1) A sample shall be selected from each wafer lot to satisfy programmability requirements. Eight devices shall be submitted to programming (see 3.2.3.1). If any device fails to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 13 total devices with no more than one total device failure allowable.

(2) For unprogrammed devices, eight devices from the programmability sample shall be submitted to the requirements of the specified tests of subgroups 1, 2, and 3 designated for programmed devices only. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 13 total devices with no more than one total device failure allowable.

(3)a Eight devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11 for binning circuit delay only. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 13 total devices with no more than one total device failure allowable.

(3)b If the binning circuit is tested on 100 percent of the products, then the above requirement is met.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall also verify functionality for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ * indicates PDA applies to subgroup 1 and 7.
5 ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{DD}	±1.0 mA
V_{OH}	±0.2 V
V_{OL}	±0.1 V
I_{OZ}	±2.0 µA
I_{OS} 2/	±5.0 mA at $V_{OUT} = V_{DD}$
	±5.0 mA at V_{OUT} = GND
t_{PBLH}, t_{PBHL}	±10 ns

1/ The above parameters shall be recorded before and after the required burn-in and life test to determine the delta.
2/ This parameter is required for devices 01 and 02 only.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein. For qualification, at least 50 percent of the sample selected for testing in subgroup 10 shall be programmed (see 3.2.3.1). For quality conformance inspection, the programmability sample (see 4.4.1f(1)) shall be included in the subgroup 1 tests of table III, method 5005 of MIL-STD-883.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Symbols, definitions, and functional descriptions. Not applicable.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 94-06-30

Approved sources of supply for SMD 5962-90965 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9096501MXX	0J4Z0	A1020A-JQ44B
5962-9096501MYX	0J4Z0	A1020A-JQ68B
5962-9096501MZX	0J4Z0	A1020A-JQ84B
5962-9096501MUX	0J4Z0 01295	A1020A-PG84B TPC1020AMGB84B
5962-9096501MTX	0J4Z0 01295	A1020A-CQ84B TPC1020AMHT84B
5962-9096501MMX	01295	TPC1020AMHFG84B
5962-9096502MXX	0J4Z0	A1020A-1-JQ44B
5962-9096502MYX	0J4Z0	A1020A-1-JQ68B
5962-9096502MZX	0J4Z0	A1020A-1-JQ84B
5962-9096502MUX	0J4Z0 01295	A1020A-1-PG84B TPC1020AMGB84B-1
5962-9096502MTX	0J4Z0 01295	A1020A-1-CQ84B TPC1020AMHT84B-1
5962-9096502MMX	01295	TPC1020AMHFG84B-1
5962-9096503MUX	0J4Z0	A1020B-PG84B
5962-9096503MTX	0J4Z0	A1020B-CQ84B
5962-9096503MMX	0J4Z0	A1020B-CQ84B
5962-9096504MUX	0J4Z0	A1020B-1PG84B
5962-9096504MTX	0J4Z0	A1020B-1CQ84B
5962-9096504MMX	0J4Z0	A1020B-1CQ84B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0J420	Actel Corporation 955 East Arques Ave. Sunnyvale, CA 94086

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. 13500 N. Central Expressway P. O. Box 655303 Dallas, TX 75265 Point of contact: 1-20 at FM 1788 Midland, TX 79711-0448

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